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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/928,848	08/13/2001	Michael I. Mandell	7784-000175	8347

27572 7590 01/27/2005

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EXAMINER	
SAXENA, AKASH	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/928,848	MANDELL ET AL.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the c ver sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 have been presented for examination based on the application filed on 13 August 2001.

Claim Interpretation

2. Claims are interpreted as follows:

Claim 1: As best understood by the examiner, the word "marker" is interpreted as "tag or compiler understood comment in a program" or "some means to point out to an compiler executing a program that some special action needs to performed at a certain point in the program wherever this tag/marker shows up".

Claim 8: As best understood by the examiner, claim 8 recites the step of "generating an output string", which is interpreted as ""generating an output string from the symbolic equation."

Information Disclosure Statement

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. *Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned.* Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information, which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by § 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and
(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

3. Information Disclosure Statement is objected to under CFR 1.56(a) as being incomplete. Examiners' inventor search found US Patent 6,757,884, (filed on 31st July, 2001), which was filed 13 days prior to current application filing date. This patent has same inventive entity & assignee and mirrors all claims except the inclusion of marker component from the current application. Examiner has cited this as reference and respectfully requests to cite any relevant patents in future.

Claim R jections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claim 1-14 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

MPEP (Chapter 2105) states that:

> If the broadest reasonable interpretation of the claimed invention as a whole encompasses a human being, then a rejection under 35 U.S.C. 101 must be made indicating that the claimed invention is directed to nonstatutory subject matter. Furthermore, the claimed invention must be examined with regard to all issues pertinent to patentability, and any applicable rejections under 35 U.S.C. 102, 103, or 112 must also be made.

The claims 1,6 & 9 do not state that the generation of symbolic equations and partitioning of the behavioral description is performed on a complex system hence a human could perform these steps manually. Also keywords like "characterizing", "creating", "generating" & "partitioning" as mentioned in the steps, could refer to a human being performing them and do not associate these steps to be performed by a computer.

Examiner respectfully suggests to include in preamble language similar to "a computer method for characterization" and in body of the claims phrases like "generating symbolical equation using a computer microprocessor", "partitioning said behavioral level description, using a microprocessor, by inserting a marker" to exclude steps that might be performed by a human being.

Claims 2-5, 7-8, 10-14 are rejected on basis their dependency upon claims 1,6 & 9 respectively.

To expedite a complete examination of the instant application the claims rejected under 35 U.S.C. § 101 (nonstatutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

"Hardware level description" can be presented on different levels of granularity, i.e., it could be a Register Transfer Logic (RTL), gate (structural) or transistor level description.

Behavioral description is a level of abstraction and so are RTL, gate & transistor. Hardware level description is a means of describing such an abstraction with increasing complexity. Applicants failed to identify which level of hardware level description is the behavioral design converted to.

Claims 2-5, 7-8, 10-14 are rejected on basis their dependency upon claims 1,6 & 9 respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. **Claim 1-4, 6, 8-9 are r ject d under 35 U.S.C. 103(a) as being unpatentable over US patent 5,933,356 issued to Rostoker in view of compiler directive commands in behavioral compiler from Synopsys[1,2,3,4].**

Regarding Claim 1

Rostoker states an electronic design (circuit) can be described using a behavioral level description (Rostoker: Col. 32 Line 31-35), which can further described inform of symbolic form (Rostoker: Col. 26 Line 56-60). He further discloses that behavioral design can be partitioned into number of blocks (Rostoker: Col. 32 Line 38-40) to meet the equivalence between the structural (hardware level description) and behavioral description (Rostoker: Col. 26 Line 48-50).

Rostoker does not state the use of a marker in partitioning the design.

Synopsys article (Doc Id 901157)[1] teaches a concept, similar in function of a marker, using compiler directives[2] in Behavioral Compiler, a Synopsys product. This article teaches how compiler directives "preserved_function" is used to set aside a section of code and implement it as described, essentially partitioning it from the rest of the code and reducing complexity. The "preserved_function" compiler directive is known to exist in 1998[3]. Also "partition_dp"[4] command can be used to do partitioning at behavioral level.

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[1] Doc Id: 901157, Product: Behavioral Compiler, Topic: "Using Preserved Functions in Behavioral Compiler"
[2] Doc Id: 002613, Product: (V)HDL Compiler, Topic: "Verilog and VHDL Directives"
[3] Doc Id: 901665, Product: Behavioral Compiler, Topic: "use_netlist attribute with preserve function"
[4] Doc Id: 901336, Product: Design Compiler, Topic: The partition_dp command does not work on a Mapped Design"

The command marker disclosed has a unique symbolic name, as multiple compiler directives can be present in a single program. The "case" construct example[5] demonstrates that multiple compiler directives can be used in the same code. It is understood that compiler will internally know how to distinguish them, hence will uniquely identify them.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to take already known teachings provided by Synopsys articles about Behavioral Compiler & Design Compiler and combine them with Rostoker's teachings to make a construct (tag/marker/directive) that will partition the behavioral model. The motivation would be the ability to partition the design so that sections of design are implemented as described and not optimized based on other constraints provided by user for the complete design. The advantage of such a decision can be apparent from modern system that contain both digital, analog and interface circuitry. Certain digital circuit architecture may be tuned to provide current or voltage drive the analog interface and should be synthesizable as digital circuit.

[5] Doc Id: 901884, Product: Design Compiler, Topic: "Case Selector Bit Ranges Not Valid"

Regarding Claim 2

Rostoker discloses that it is well known in the art that after the code is compiled output variables can be expressed in form of input variables. (Rostoker: Col.7 Lines 6-12).

Regarding Claim 3

Rostoker discloses that it is well known in the art that, functional verification between behavioral and structural (HDL) descriptions can both be done with number as well as symbolic inputs (files) for the proof of equivalence (Rostoker: Col.26 Lines 48-51, 56-62).

Regarding Claim 4

As disclosed in claim 1, Synopsys articles teach multiple compiler directives can be present in a program. Hence, it is known in the art that in such a scenario each one must be given a unique symbolic name for compiler to differentiate.

Regarding Claim 6

Claim 6 is rejected for the same reasons as claims 1 & 4 are rejected.

Regarding Claim 8

Rostoker also disclose that a netlist file generated from the design that can be used to generate output string mapped in terms of input path (Rostoker: Col.6 Lines 43-45, Col.7 Lines 6-11).

Regarding Claim 9

Claim 9 is rejected for the same reasons as claim 1 is rejected.

Regarding Claim 5 & 7

Claim 5 & 7 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

7. **Claim 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent 5,933,356 issued to Rostoker in view of compiler directive commands in behavioral compiler from Synopsys further in view of US Patent 6,182,258 issued to Hollander.**

Regarding Claim 10,11,12,13 &14

Rostoker disclosed that it is well known in the art how to generate the symbolic, numeric & hardware descriptive language descriptions of the behavioral description and to prove their equivalence using a theorem prover (Rostoker: Col.26 Lines 48-51, 56-62).

Rostoker does not teach that these descriptions are modeled in C language.

Hollander teaches that verification & modeling can be done in C language because C models are faster than HDL model for doing verification. (Hollander: Col.1 Lines 55-61, Col.2 Lines 50-57).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to use the teachings of Hollander to model the symbolic, numeric and HDL descriptions in the C language. The motivation would be faster simulation time, richer syntax and verification tools, that would allow an

accurate modeling of the behavioral description. Further, same stimulus file can be used for all three models to verify the functionality.

Other Art cited but not used:

1. *"Computer-Aided Partitioning of Behavioral Hardware Descriptions"* by Michael C McFarland, S.J., sites the concerns related to partitioning a behavioral model in the absence of data paths allocations and basis of such partitioning. He further describes metrics, qualitative & quantitative analysis between methods of partitioning and equivalence.
2. "Assignment Decision Diagram for High Level Synthesis" by Chaiyakul & Gajski, details how a behavioral description can be represented in partially unique hardware descriptive language (HDL), irrespective of way the description is provided. It details how different constructs implied in the behavioral description are transformed/synthesized into HDL through decomposition. This decomposition has intermediate marker like characteristics described by the inventor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 8:30 - 5:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on (571)272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

as

JEAN B. HOMERE
PRIMARY EXAMINER